AMENDMENTS TO THE CLAIMS

Claims 1-17 (Cancelled)

18. (Original) A memory device comprising:

a muxing device; and

at least one cluster device coupled to said muxing device.

19. (Currently Amended) The memory device of Claim 18, wherein said cluster device is adapted to sink a tail current of at least one~~all~~ local sense ~~amps~~amp contained in said cluster device.

20. (Currently Amended) The memory device of Claim 18, further comprising a plurality of local cluster~~s~~ devices having ~~a~~ at least one common local wordline coupling all said cluster~~s~~ devices in a block.

21. (Currently Amended) The memory device of Claim 18, wherein said cluster device comprises at least one sense ~~amplifier~~ amp adapted to be activated by a global cluster line.

22. (Cancelled)

23. (Original) A sense amplifier device having at least one sense amplifier and adapted to be used in a memory device comprising:

a precharging and equalizing device adapted to precharge and equalize unused lines at a predetermined value; and

at least one transistor adapted to isolate the sense amplifier.

24. (Currently Amended) The sense amplifier device of Claim ~~13~~23, further comprising at least one PMOS transistor adapted to isolate the sense amplifier from a global bit line.

Claims 25-26 (Cancelled)

27. (New) The memory device of Claim 18, wherein said cluster device is adapted to sink a tail current of all local senses amps contained in said cluster device.

28. (New) The memory device of Claim 18, wherein said cluster device is a self-timed local element interfacing with at least said muxing device.

29. (New) The memory device of Claim 18 comprising at least one global cluster line and at least one local cluster line.

30. (New) The memory device of Claim 18 comprising at least one local cluster line coupled to at least one local sense amplifier in said cluster device.

31. (New) The memory device of Claim 18 wherein said at least one cluster device comprises an array of local sense amplifiers.

32. (New) The memory device of Claim 31 wherein said array of local sense amplifiers comprises four pairs of bitline multiplixers.

33. (New) The memory device of Claim 32 wherein each bitline multiplixer connects at least one bitline pair to a global bitline.

34. (New) A memory device comprising:

a plurality of muxing devices;

a plurality of cluster devices interfacing with at least one of said plurality of muxing devices; and

at least one common local wordline coupling said plurality of cluster devices in a block.

35. (New) The memory device of Claim 34, wherein said cluster device is adapted to sink a tail current of at least one local sense amp contained in at least one of said cluster devices.

36. (New) The memory device of Claim 34, wherein said cluster device comprises at least one sense amplifier adapted to be activated by a global cluster line.

37. (New) The memory device of Claim 34, wherein said cluster device is a self timed local element interfacing with at least one of said muxing devices.

38. A method of performing at least one of a read and write operation in a memory device comprising:

activating at least one cluster device in the memory device; and

firing at least one sense amp in said at least one cluster device.

39. The method of Claim 38 wherein at least one global cluster line is activated prior to said at least one of a read and write operation.

40. The method of Claim 39 wherein said global cluster line is activated by an external interface to at least one of said cluster devices involved in said at least one of a read and write operation.

41. The method of Claim 38 comprising sinking a tail current of at least one local sense amp contained in said cluster device.

42. The method of Claim 38 comprising firing all said sense amps in said at least one cluster device.